0.1 GHz to 33 GHz,1 dB LSB, 5-Bit, GaAs Digital Attenuator

Data Sheet **HMC939ATCPZ-EP**

FEATURES

- Attenuation range: 1 dB LSB steps to 31 dB
- Insertion loss: 6 dB typical at 33 GHz
- Attenuation accuracy: ±0.5 dB
- Input linearity
  - 0.1 dB compression (P0.1dB): 24 dBm typical
  - 3rd-order intercept (IP3): 40 dBm typical
- Power handling: 27 dBm maximum
- Dual-supply operation: ±5 V
- CMOS-/TTL-compatible parallel control
- 24-lead, 4 mm × 4 mm LFCSP package

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Test instrumentation
- Microwave radios and very small aperture terminals (VSATs)
- Military radios, radars, electronic counter measures (ECMs)
- Broadband telecommunications systems

FUNCTIONAL BLOCK DIAGRAM

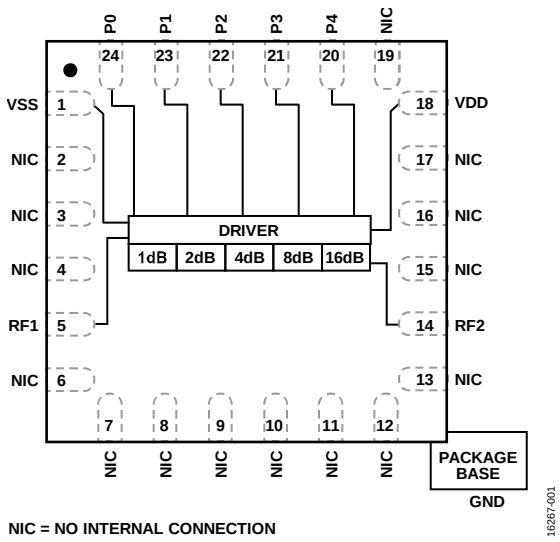


Figure 1.

GENERAL DESCRIPTION

The HMC939ATCPZ-EP is a 5-bit digital attenuator with a 31 dB attenuation control range in 1 dB steps.

The HMC939ATCPZ-EP offers optimum insertion loss, attenuation accuracy, and input linearity over the specified frequency range from 100 MHz to 33 GHz.

The HMC939ATCPZ-EP requires dual-supply voltages, V_{DD} = 5 V and V_{SS} = −5 V, and provides a complementary metal oxide semiconductor (CMOS)-/transistor to transistor level (TTL)-compatible parallel control interface by incorporating an on-chip driver.

The HMC939ATCPZ-EP comes in a RoHS compliant, compact, 4 mm × 4 mm LFCSP package.

Additional application and technical information can be found in the HMC939ALP4E data sheet.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

10/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V, V_{SS} = −5 V, V_{Px} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.1		33	GHz
INSERTION LOSS		0.1 GHz to 18 GHz		4.5	5.5	dB
		18 GHz to 26.5 GHz		5.5	7.0	dB
		26.5 GHz to 33 GHz		6	8	dB
ATTENUATION						
Range		Between minimum and maximum attenuation states, 0.1 GHz to 33 GHz		31		dB
Step Size		Between any successive attenuation states, 0.1 GHz to 33 GHz		1		dB
Step Error		Between any successive attenuation states, 0.1 GHz to 33 GHz		0.5		dB
State Error		Referenced to insertion loss state				
		1 dB to 15 dB attenuation states, 0.1 GHz to 33 GHz	−(0.5 + 5% of attenuation state)		+(0.5 + 5% of attenuation state)	dB
		16 dB to 31 dB attenuation states, 0.1 GHz to 20 GHz	−(0.5 + 5% of attenuation state)		+(0.5 + 5% of attenuation state)	dB
		16 dB to 31 dB attenuation states, 20 GHz to 33 GHz	−(0.6 + 8% of attenuation state)		+(0.6 + 8% of attenuation state)	dB
RETURN LOSS		RF1 and RF2 pins, all attenuation states, 0.1 GHz to 33 GHz		10		dB
RELATIVE PHASE		Between minimum and maximum attenuation states				
		0.1 GHz to 18 GHz		45		Degrees
		18 GHz to 26.5 GHz		60		Degrees
		26.5 GHz to 33 GHz		80		Degrees
SWITCHING CHARACTERISTICS		Between all attenuation states				
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of radio frequency (RF) output		45		ns
On and Off Time	t_{ON}, t_{OFF}	50% digital control input voltage (V_{CTL}) to 90% of RF output		60		ns
INPUT LINEARITY		All attenuation states				
0.1 dB Compression	P0.1dB	0.1 GHz to 0.5 GHz		20		dBm
		0.5 GHz to 33 GHz		24		dBm
Third-Order Intercept	IP3	8 dBm per tone, 1 MHz spacing				
		0.1 GHz to 0.5 GHz		43		dBm
		0.5 GHz to 33 GHz		40		dBm
SUPPLY CURRENT						
Positive	I_{DD}		2.5	4.5	6.5	mA
Negative	I_{SS}		−7.0	−5.5	−3.0	mA
DIGITAL CONTROL INPUTS		P0 to P4 pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		2		5	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	
Positive	7 V
Negative	−7 V
Digital Control Input Voltage, V_{CTL}	V_{DD} + 0.5 V
RF Input Power (All Attenuation States, f = 0.1 GHz to 33 GHz, T_{CASE} = 85°C)	27 dBm
Continuous Power Dissipation, P_{DISS}	
(T_{CASE} = 85°C)[1]	0.453 W
(T_{CASE} = 105°C)[1]	0.314 W
(T_{CASE} = 125°C)[1]	0.174 W
Temperature	
Junction, T_J	150°C
Case, T_{CASE}	−55°C to +125°C
Storage	−65°C to +150°C
Reflow[2] Moisture Sensitivity Level 3 (MSL3) Rating	260°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

[1] See Figure 2.
[2] See the Ordering Guide for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-22[1]	213	143.5[2]	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.
[2] The device is set to maximum attenuation state.

POWER DERATING CURVE

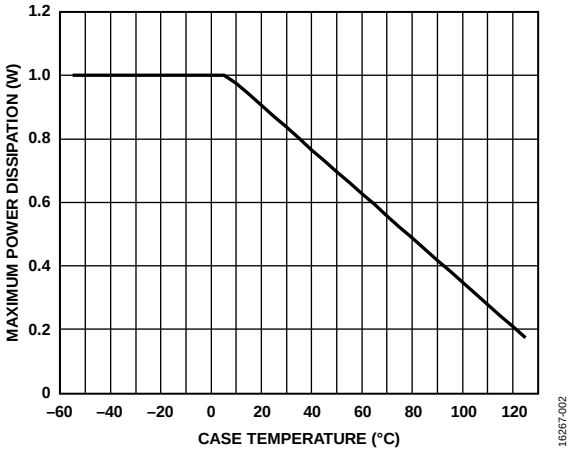


Figure 2. Maximum Power Dissipation vs. Case Temperature (T_{CASE})

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

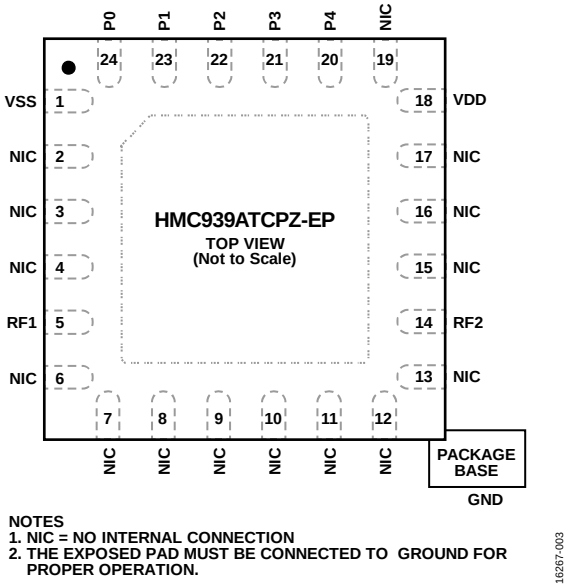


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VSS	Negative Supply Voltage.
2 to 4, 6 to 13, 15 to 17, 19	NIC	Not Internally Connected. These pins are not internally connected; however, all data shown herein was measured with these pins connected to the RF/dc ground of evaluation board.
5, 14	RF1, RF2	RF Inputs or Outputs of Attenuator. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
18	VDD	Positive Supply Voltage.
20 to 24	P4 to P0	Parallel Control Voltage Inputs. These pins select the required attenuation. There is no internal pull-up or pull-down resistor on these pins; therefore, they must always be kept at a valid logic level (V_{INH} or V_{INL}) and not be left floating.
	EPAD	Exposed Pad. The exposed pad must be connected to ground for proper operation.

Table 5. P4 to P0 Truth Table

Digital Control Input[1]					Attenuation
P4	P3	P2	P1	P0	State (dB)
High	High	High	High	High	0 dB (reference)
High	High	High	High	Low	1 dB
High	High	High	Low	High	2 dB
High	High	Low	High	High	4 dB
High	Low	High	High	High	8 dB
Low	High	High	High	High	16 dB
Low	Low	Low	Low	Low	31 dB

[1] Any combination of the control voltage input states shown in Table 5 provides an attenuation equal to the sum of the bits selected.

INTERFACE SCHEMATICS

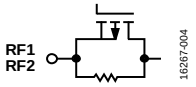


Figure 4. RF1 and RF2 Interface Schematic

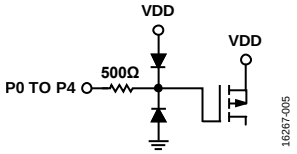


Figure 5. Parallel Control Voltage Inputs Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

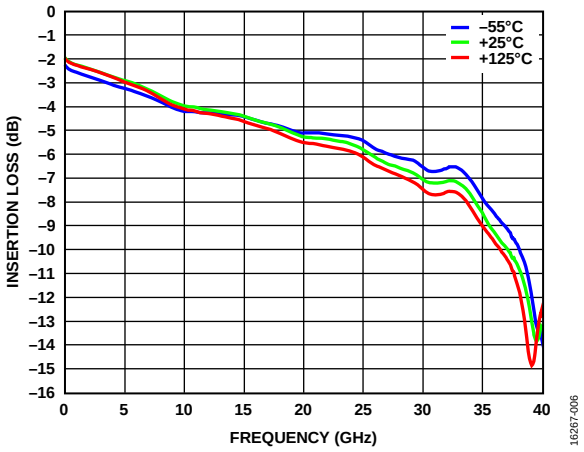


Figure 6. Insertion Loss vs. Frequency at Various Temperatures

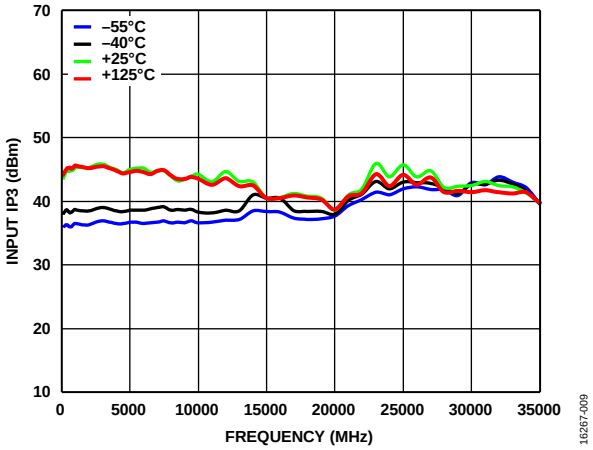


Figure 9. Input IP3 vs. Frequency at Minimum Attenuation State and at Various Temperatures

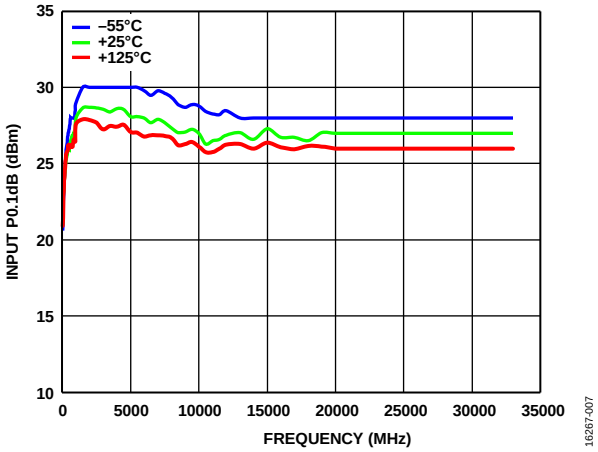


Figure 7. Input P0.1dB vs. Frequency at Minimum Attenuation State and at Various Temperatures

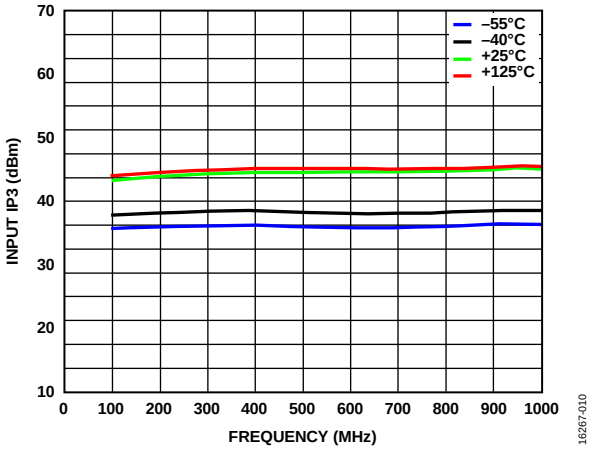


Figure 10. Input IP3 vs. Frequency at Minimum Attenuation State and at Various Temperatures (Low Frequency Detail)

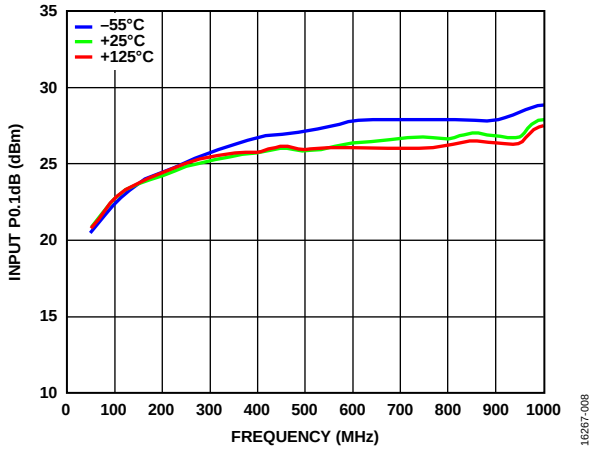
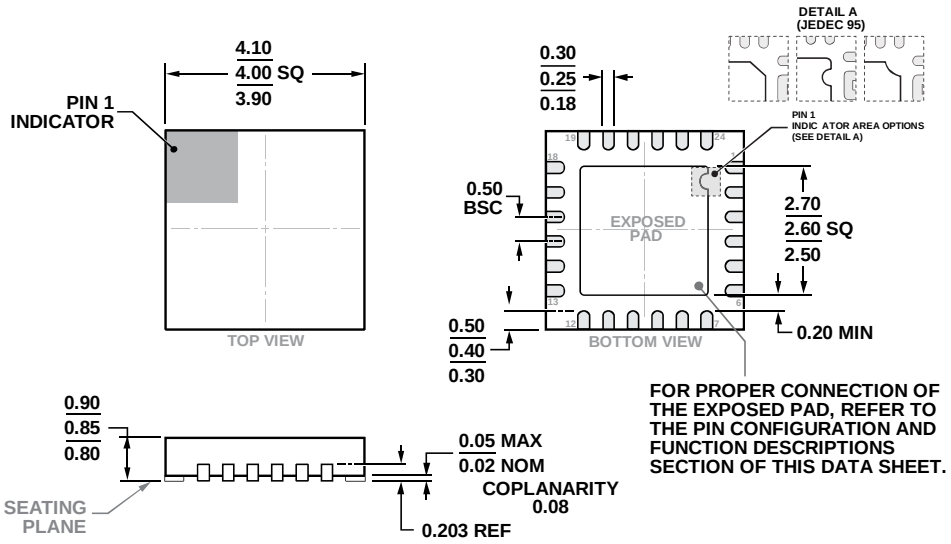


Figure 8. Input P0.1dB vs. Frequency at Minimum Attenuation State and at Various Temperatures (Low Frequency Detail)

OUTLINE DIMENSION



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.

Figure 11. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.85 mm Package Height
(CP-24-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC939ATCPZ-EP-PT	−55°C to +125°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-22
HMC939ATCPZ-EP-R7	−55°C to +125°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-22

[1] All models are RoHS compliant devices.
[2] See the Absolute Maximum Ratings section.